Customer No.: 31561
Docket No.: 13041-US-PA
Application No.: 10/710,732

REMARKS

Present Status of the Application

The Office Action rejected claims 1-20 under 35 U.S.C. 102(e), as being anticipated by Rhodes (US 6,856,001).

No claim is amended. Claims 1-20 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Office Action Rejections

Applicants respectfully traverse the 102(e) rejection of claims 1-20 because Rhodes (US 6,856,001) does not teach every element recited in these claims.

In order to properly anticipate Applicants' claimed invention under 35 U.S.C 102, each and every element of claim in issue must be found, "either expressly or inherently described, in a single prior art reference". "The identical invention must be shown in as complete details as is contained in the .... claim. Richardson v. Suzuki Motor Co., 868 F. 2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)." See M.P.E.P. 2131, 8th ed., 2001.

The present invention is in general related to a method of fabricating a photodiode as claim 1 recites:

> Claim 1. A method of fabricating a photodiode, comprising the steps of:
> providing a substrate;
> forming a well region of a first conductive type in the substrate;

forming an isolation structure in the substrate to define a photosensitive area on the substrate;

forming a plurality of trenches in the well region of the substrate within the photosensitive area; and

forming a doped layer of a second conductive type over the substrate, wherein the doped layer covers the interior walls of the trenches and the surface of the substrate within the photosensitive area.

Rhodes fails to teach or suggest that a doped layer of a second conductive type is formed covering the interior walls of the trenches and the surface of the substrate within the photosensitive area as claim 1 recites. In the Rhodes's reference, the process shown in Figs. 1-8 is a method for forming an isolation structure, and Fig. 9 shows an integrated circuit with the isolation structure of Fig. 8. Rhodes teaches forming a trench 22 in the well 13 and then filling an oxide layer 34 in the trench 22 (Fig. 6) after forming a dielectric layer 24 (Fig. 3) and performing an ion implanting process (Fig. 5) so as to form an isolation region 36 (Figs 7 and 8). The isolation regions 46A, 46B shown in Fig. 9 are formed by the method of Figs. 1-8. The impurity-doped regions 52, 53 shown in Fig. 9 are used as a source and a drain.

The Office Action points out that a doped layer of a second conductive type covering the interior walls of the trenches and the surface of the substrate within the photosensitive area recited in claim 1 is as the references 52, 53. But Applicants do not agree. This is because the impurity-doped regions 52, 53 are not formed in the trenches. Moreover, the impurity-doped regions 52, 53 do not cover the interior walls of the trenches and the surface of the substrate within the photosensitive area. The method disclosed by the citation is for forming an isolation

structure, but the method of claim 1 is for forming a photodiode. Rhodes does not teach forming a photodiode in the trenches. Thus, Rhodes fails to teach every element in claim 1.

Therefore, Applicants respectfully submit that independent claim 1 patently defines over the prior art reference, and should be allowed. For at least the same reasons, dependent claims 2-15 patently define over the prior art as a matter of law, for at least the reason that these dependent claims contain all features of independent claim 1.

The present invention also provides anther method of fabricating a photodiode as claim 16 recites:

> Claim 16. A method of fabricating a photodiode, comprising the steps of:
> providing a substrate;
> forming a well region of a first conductive type in the substrate;
> forming an isolation structure in the well region of the substrate to define a photosensitive area on the substrate;
> forming a plurality of trenches in the substrate within the photosensitive area;
> ***forming a buffer layer over the substrate, wherein the buffer layer covers the interior walls of the trenches and the surface of the substrate within the photosensitive area;***
> forming a doped layer of a second conductive type over the buffer layer; and
> ***performing an annealing operation to drive dopants within the doped layer into the buffer layer and form a junction of the second conductive type and the first conductive type within the buffer layer.***

Rhodes fails to teach or suggest that a buffer layer is formed covering the interior walls of the trenches and the surface of the substrate within the photosensitive area as claim 16 recites. The Office Action points out that the reference 14 of Fig. 1 in the citation is the buffer layer as claim 16 recites. However, the reference 14 of Fig. 1 in the citation is a pad oxide layer, and the

pad oxide layer 14 and the substrate 12 are etched to form a trench 22 (col. 3, lines 41-51). Therefore, the layer 14 does not cover the interior walls of the trench and the surface of the substrate. In addition, in claim 16, the buffer layer is formed covering the interior walls of the trenches, and a doped layer of a second conductive type is formed over the buffer layer. Hence, the doped layer of the second conductive type is also formed in the trench. But, in Rhodes's reference, the reference 54 of Fig. 9 is not formed in the trench.

Rhodes also fails to teach or suggest that dopants within the doped layer are driven into the buffer layer to form a junction of the second conductive type and the first conductive type within the buffer layer as claim 16 recites. The Office Action points out that Rhodes has disclosed said limitation at col. 5, lines 27-33. However, Applicants do not agree. Rhodes discloses, at col. 5, lines 27-33, ions are implanted beneath the partially-filled trenches 22 as shown in Fig. 4, and a CVD oxide 34 is deposited to fill the trenches completely as shown in Fig. 6. After deposition of the CVD oxide 34, an anneal process can be performed to density the oxide and activate the field implants (col. 5, lines 27-33). In other words, the anneal process disclosed by Rhodes can density the oxide and activate the field implant. But, Rhodes does not teach dopants within the doped layer are driven into the buffer layer to form a junction of the second conductive type and the first conductive type within the buffer layer.

For at least the foregoing reasons, Applicants respectfully submit that independent claim 16 patently defines over the prior art reference, and should be allowed. For at least the same reasons, dependent claims 17-20 patently define over the prior art as well.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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Respectfully submitted,

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